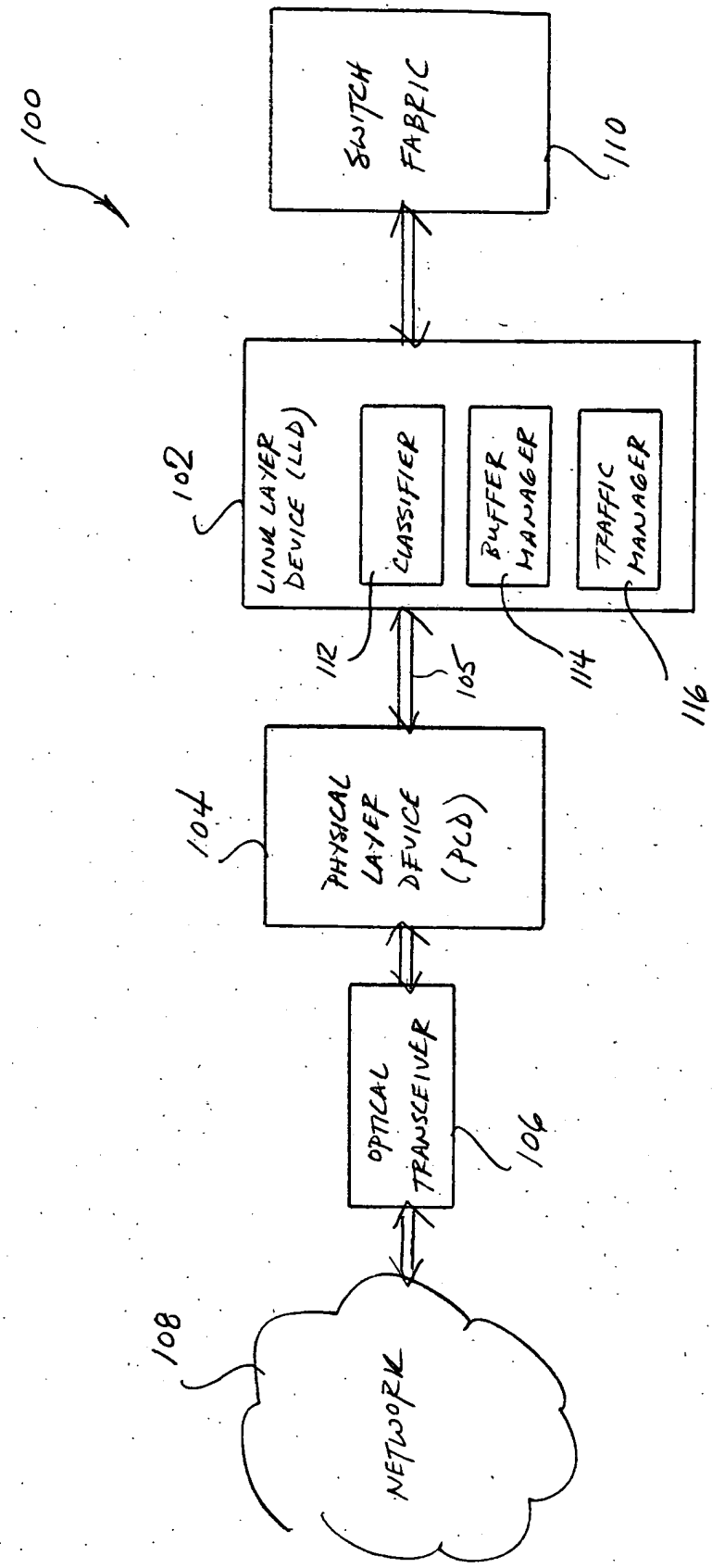
100
SWITCH FABRIC
110
LINK LAYER DEVICE (LLD)
102
CLASSIFIER
BUFFER MANAGER
TRAFFIC MANAGER
112
105
114
116
PHYSICAL LAYER DEVICE (PLD)
104
OPTICAL TRANSCEIVER
106
NETWORK
108

FIG. 1

F	A	C	I	FCS	F

Field Name	Size (bits)
Flag Field (F)	8 bits
Address Field(A)	8 bits
Control Field (C)	8 or 16 bits
Information Field (I)	Variable
Frame Check Sequence (FCS)	16 or 32 bits

FIG. 2

	Packet Overhead (assuming max size FOH = 8B)			
	FOH	SOH	PS	% OH
No Stuffing, min sized packet	8	0	40	**20%**
Max Stuffing, min sized packet	8	8	40	**40%**
No Stuffing, max sized packet	8	0	9600	**0.08%**
Max Stuffing, max sized packet	8	1920	9600	**20%**

Assumptions:

a) Packet Size (**PS**):
40 – 9600 bytes

b) Worst-case HDLC bit stuffing overhead (**SOH**)
20% of (a) = 8 – 1920 bytes

c) HDLC Frame Overhead (**FOH**)
5 – 8 bytes

FIG. 3

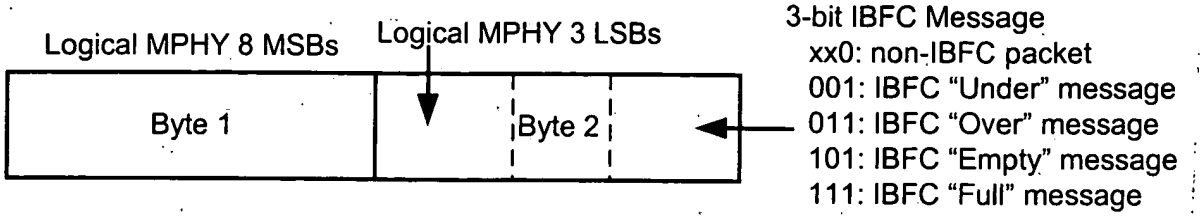
Logical MPHY 8 MSBs
Logical MPHY 3 LSBs
Byte 1
Byte 2
3-bit IBFC Message
xx0: non-IBFC packet
001: IBFC "Under" message
011: IBFC "Over" message
101: IBFC "Empty" message
111: IBFC "Full" message

FIG. 4

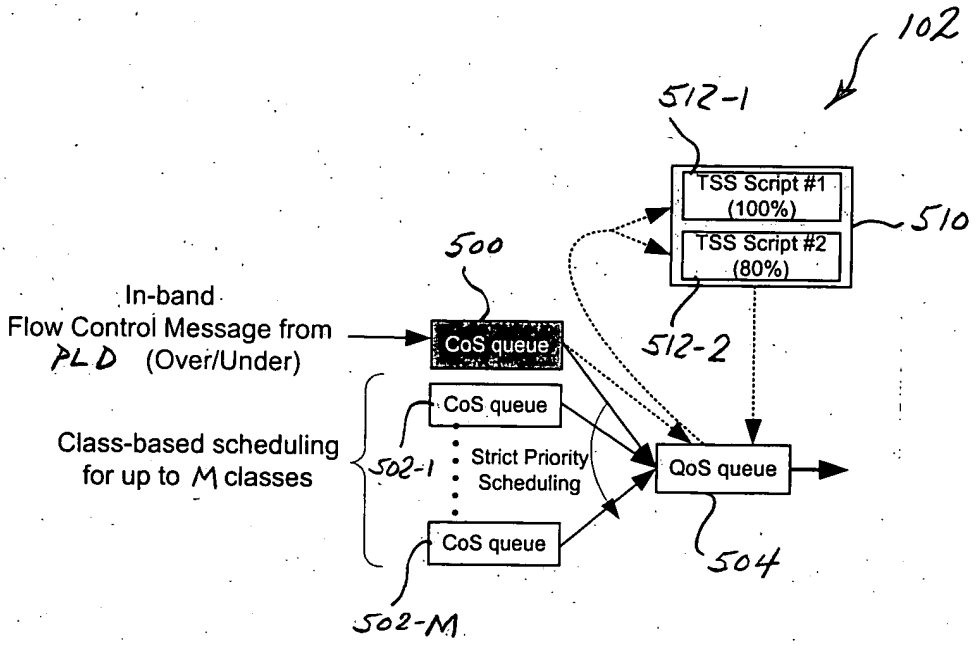
102
512-1
TSS Script #1 (100%)
TSS Script #2 (80%)
510
500
In-band Flow Control Message from PLD (Over/Under)
CoS queue
512-2
CoS queue
Class-based scheduling for up to M classes
502-1
Strict Priority Scheduling
QoS queue
CoS queue
504
502-M

FIG. 5

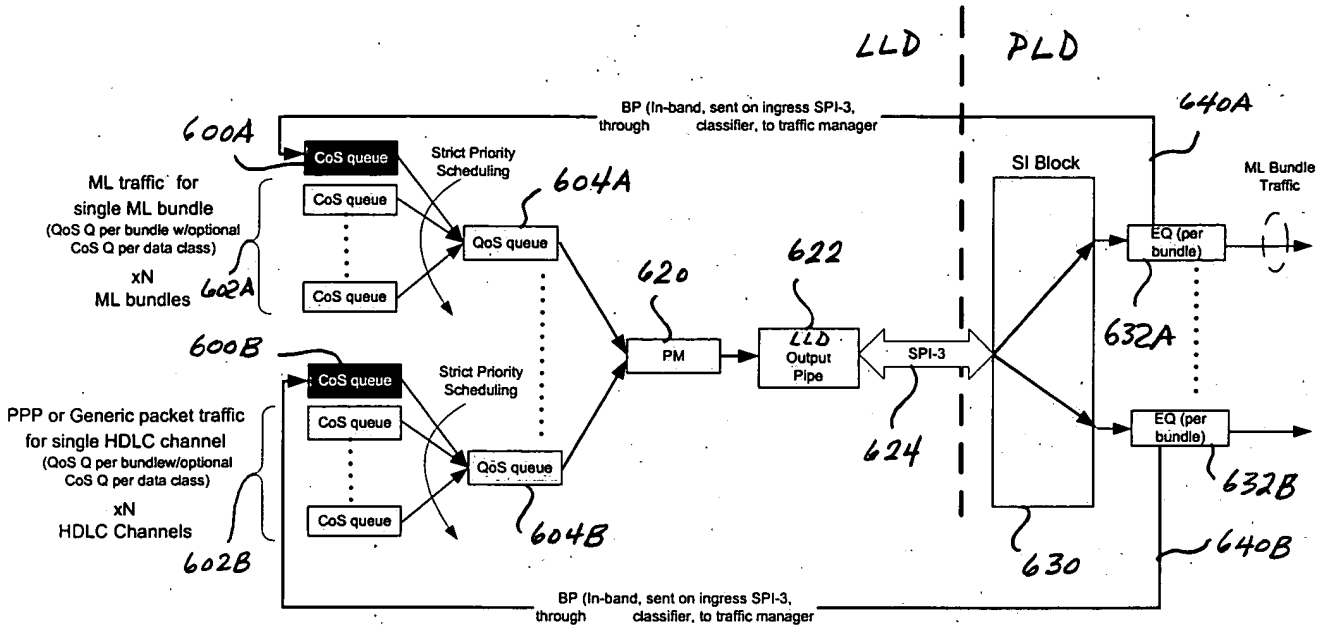
LLD
PLD
600A
CoS queue
Strict Priority Scheduling
604A
ML traffic for single ML bundle
(QoS Q per bundle w/optional CoS Q per data class)
xN ML bundles
602A
CoS queue
QoS queue
CoS queue
BP (In-band, sent on ingress SPI-3, through classifier, to traffic manager
640A
SI Block
ML Bundle Traffic
620
622
PM
LLD Output Pipe
SPI-3
EQ (per bundle)
632A
600B
CoS queue
Strict Priority Scheduling
PPP or Generic packet traffic for single HDLC channel
(QoS Q per bundlew/optional CoS Q per data class)
xN HDLC Channels
602B
CoS queue
QoS queue
CoS queue
604B
624
EQ (per bundle)
632B
630
640B
BP (In-band, sent on ingress SPI-3, through classifier, to traffic manager

FIG. 6

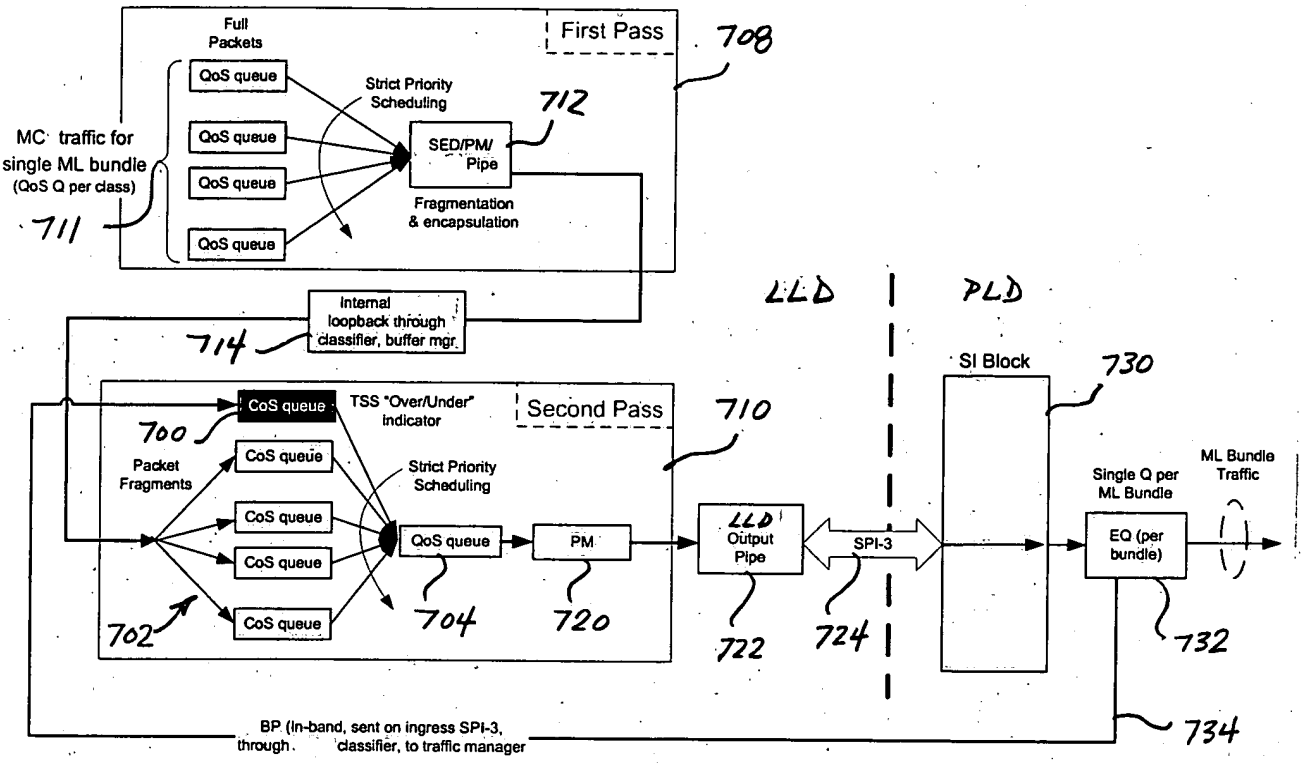
Full Packets
First Pass
708
QoS queue
QoS queue
QoS queue
QoS queue
Strict Priority Scheduling
712
SED/PM/ Pipe
Fragmentation & encapsulation
MC traffic for single ML bundle (QoS Q per class)
711
LLD
PLD
Internal loopback through classifier, buffer mgr.
714
SI Block
730
CoS queue
TSS "Over/Under" indicator
Second Pass
710
700
CoS queue
Packet Fragments
Strict Priority Scheduling
CoS queue
CoS queue
QoS queue
PM
LLD Output Pipe
SPI-3
Single Q per ML Bundle
EQ (per bundle)
ML Bundle Traffic
CoS queue
702
704
720
722
724
732
BP (In-band, sent on ingress SPI-3, through classifier, to traffic manager
734

FIG. 7

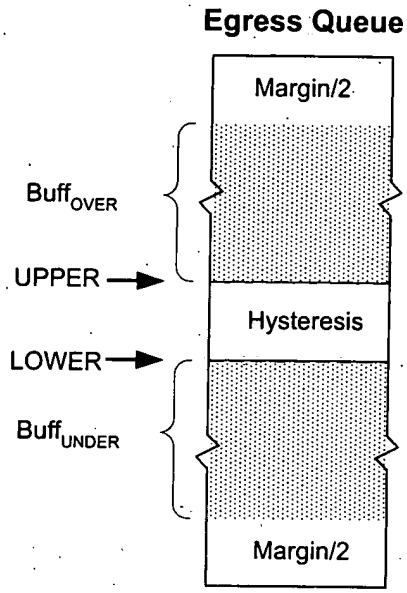
Egress Queue
Margin/2
Buff$_{OVER}$
UPPER
Hysteresis
LOWER
Buff$_{UNDER}$
Margin/2

FIG. 8

Parameter Definitions	
R_{PORT} : Nominal data rate of a PLD HDLC channel corresponding to an EQ. R_{FILL} : Data input (equeue) rate of PLD EQ. R_{DRAIN} : Data output (dequeue) rate of PLD EQ. FCL : Flow control latency.	D_{MTU} : Delay due to transmission of an MTU-sized packet from LLD CoS queue. D_{LLD} : Worst-case classification delay of LLD. D_{PIPE} : Output pipeline delay of LLD. D_{PLD} : PLD delay in transmitting IBFC message.

$$Buff = |R_{FILL} - R_{DRAIN}| * FCL$$

$$|R_{FILL} - R_{DRAIN}| = |R_{PORT} - 0.8R_{PORT}| = 0.2 * R_{PORT}\ ^{\dagger}$$

$$FCL = D_{MTU} + D_{LLD} + D_{PIPE} + D_{PLD}\ ^{\ddagger}$$

Use the following facts and worst-case assumptions:

$$D_{MTU\text{-}L} = MTU \div (0.8 * R_{PORT}); \quad D_{MTU\text{-}U} = MTU \div R_{PORT}$$

$$D_{LLD} \le 20\ \mu sec.\ ^{\dagger\dagger}$$

$$D_{PIPE} \le 6\ \mu sec.\ ^{\ddagger\ddagger}$$

$$D_{PLD} \le 1\ \mu sec.\ ^{\S}$$

$$Buff_{UNDER} = (0.2 * R_{PORT}) * ([MTU / (0.8 * R_{PORT})] + 20\ \mu s + 6\ \mu s + 1\ \mu s)$$

$$= (0.2 * R_{PORT}) * ([MTU / (0.8 * R_{PORT})] + 27\ \mu s)$$

$$= R_{PORT} * ([0.25 * MTU / R_{PORT})] + 5.4\ \mu s)$$

$$= (0.25 * MTU) + (R_{PORT} * 5.4\ \mu s)$$

$$Buff_{OVER} = (0.2 * R_{PORT}) * ([MTU / R_{PORT}] + 20\ \mu s + 6\ \mu s + 1\ \mu s)$$

$$= (0.2 * R_{PORT}) * ([MTU / R_{PORT}] + 27\ \mu s)$$

$$= R_{PORT} * ([0.2 * MTU / R_{PORT})] + 6.75\ \mu s)$$

$$= (0.2 * MTU) + (R_{PORT} * 6.75\ \mu s)$$

† HDLC R_{DRAIN} is at most 20% greater or less than scheduler R_{FILL}

‡ Flow_Control_Latency is equal to the sum of the delays (D) shown

†† W.C. delay of the flow control message through classification to the traffic shaper

‡‡ LLD output pipeline delay

§ W.C. delay from flow control message generation in PLD to transmission on the SPI-3 ingress interface

FIG. 9

HDLC Channel Size	HDLC Channel Rate (in Kbps)	MTU (in bytes)	$Buff_{UNDER}$ (in bytes)	$Buff_{OVER}$ (in bytes)	Lower bound EQ Size (in bytes)	Worst-case EQ Size (in bytes)
DS0	64	576	145	116	261	586
	64	1518	380	304	684	1432
	64	9600	2401	1921	4322	8708
DS1	1544	576	146	117	263	590
	1544	1518	381	305	686	1436
	1544	9600	2402	1922	4324	8712
8 x DS1	12352	576	153	126	279	622
	12352	1518	388	315	703	1470
	12352	9600	2409	1931	4340	8744

FIG. 10